Design of a Mixed Prime Factor FFT for Portable Digital Radio Mondiale Receiver

Dong-Sun Kim, Member, IEEE, Sang-Seol Lee, Jae-Yeon Song, Kyu-Yeul Wang, and Duck-Jin Chung

Abstract — To achieve better sound quality and to improve data reception, digital radio mondiale (DRM) offers a worldwide initiative to bring analog amplitude modulation (AM) radio into the digital era. DRM systems use coded orthogonal frequency division multiplexing (COFDM) modulation with a multilevel coding scheme to get high resistance to the multipath padding and interference. The bandwidth of a DRM passband signal is less than 20 kHz and the number of carriers used in orthogonal frequency division multiplexing (OFDM) modulation is relatively small. For this reason, DRM systems use non-power-of-two Fast Fourier Transforms (FFT) for OFDM demodulation, such processing gives way to more speed and power consumption in critical paths in DRM receivers. In this paper, we propose a mixed radix-2 and prime factor FFT algorithm for portable DRM receivers. Using the proposed architecture, we can reduce the processing time and energy consumption compared to conventional digital signal processor (DSP) based DRM receivers.

Index Terms — Digital radio mondiale, prime factor fast fourier transform, orthogonal frequency division multiplexing.

I. INTRODUCTION

With the development of multimedia technology, the desire for high quality audio and video services has rapidly increased. Many researchers have met these needs [1], [2], and several universal standards have been proposed [3], [4]. The digital radio mondiale (DRM) is a digital broadcasting system for long, medium, and short-wave bands for the radio frequencies below 30 MHz. DRM has been standardized by the European Telecommunication Standards Institute as ETSI ES 201 980 [4]. A DRM system uses existing amplitude modulation (AM) broadcast frequency bands and it is designed to fit with a 9 kHz or 10 kHz bandwidth. Additionally, four transmission modes and different system bandwidths have been defined to permit broadcasting with variable channelization constraints and propagation conditions. Besides the nominal bandwidths of 9/10 kHz, the system also supports also half channel modes (4.5 and 5 kHz) to allow for simulcast with analog AM as well as double channel modes (18 and 20 kHz) where design constraints allow for such facility resulting in larger capacity. The trade-off between capacity and ruggedness to noise, multipath spread and Doppler spread can be defined by the constellation, code rate and the orthogonal frequency division multiplexing (OFDM) mode. Considering all the parameters, a typical data rate in the 9kHz or 10 kHz channels is between 20–24 kbit/s, the maximum data rate in a 20 kHz channel is 72 kbit/s [1], [5]. As shown in Fig. 1, DRM provides the opportunity to deliver a new range of both audio and data services using existing and new transmission infrastructure in current AM frequency allocations. The DRM system uses coded orthogonal frequency division multiplex (COFDM) for digital broadcasting over AM bands. All the data produced from the digitally encoded audio and associated data signals are shared for transmission across a large number of closely spaced carriers. All of these carriers are contained within an allotted transmission channel and time interleaving is applied in order to mitigate fading. DRM system parameters are selected to allow transmission to be designed to find the best combination of transmit power, robustness, and data capacity [5]. Most of the computation power is used in the COFDM demodulation to compute Fast Fourier Transforms (FFT) and Inverse Fast Fourier Transforms (IFFT) on complex samples. Because the bandwidth of a DRM passband signal is less than 20 kHz and the number of carriers used in the OFDM modulation is relatively small, FFT for OFDM demodulation has to be performed on non-power-of-two numbers of samples, which is rare in the signal processing field [6], [7]. DRM systems use 4 different modes and each mode has different FFT size as shown in Table I. An FFT the size of mode B can be replaced by a power-of-two FFT and the other modes need non-power-of-two FFT. For the implementation of FFT algorithms, common factor algorithms and prime factor algorithms are commonly used. These algorithms are distinguished by the scheme in which two input sequences are decomposed. The radix-2 FFT algorithm takes two data points concurrently from.
memory and performs butterfly computations. This procedure is repeated \(N \log_2 N/2\) times in an \(N\)-point Discrete Fourier Transform (DFT). Butterfly computations require twiddle factors at various stages in either natural or bit-reversed order. In this paper, we propose a new FFT architecture that combines prime factor FFT with modified radix-2\(N\) FFT in order to reduce processing time and energy consumption. The proposed hybrid prime factor FFT architecture uses two-dimensional index mapping and a reusing technique to reduce the complexity of the multiplier and twiddle factor.

The rest of this paper is organized as follows. Section II explains the hybrid prime factor FFT for DRM systems. Implementation results are discussed in section III, and the conclusions are presented in section IV.

### Table I

<table>
<thead>
<tr>
<th>Mode</th>
<th>FFT Size</th>
<th>Used carriers (In 10kHz channel)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>288</td>
<td>226</td>
</tr>
<tr>
<td>B</td>
<td>256</td>
<td>206</td>
</tr>
<tr>
<td>C</td>
<td>176</td>
<td>138</td>
</tr>
<tr>
<td>D</td>
<td>112</td>
<td>88</td>
</tr>
</tbody>
</table>

II. PRIME FACTOR FFT FOR OFDM DEMODULATION IN DRM RECEIVERS

The OFDM technique divides the data into several frequency sub-channels whose bandwidth is less than the total data rate [7]. A conventional OFDM system is represented in Fig. 2, and Fig. 3 shows a DRM system using OFDM technique. The key part to an OFDM receiver is the FFT for multicarrier demodulation, and the computational complexity is proportional to the square of the FFT size. To reduce the complexity of implementation and it is desirable to convert the calculation of a long DFT into short DFTs, various decomposition algorithms have been proposed [8], [9]. For a radix-2 FFT calculation, a number of radix-2 DFTs are formed by decomposing a long DFT using common factor mapping (CFM). But the CFM method generates a large number of twiddle factors and requires numerous multiplication operations. To eliminate the requirement for twiddle factor multiplication, prime factor mapping (PFM) can be used for the decomposition if the composite factors of the sequence length of the DFT are prime numbers [10]. For using PFM method, it is necessary to define the index mappings of the DFT form. If \(N_1\) and \(N_2\) are relatively prime \((N = N_1N_2)\), a different choice of the constants can be selected to eliminate the twiddle factors as shown in Table II. Equation (1) shows the relation of the twiddle factor and the index mapping; it requires that \(((AC))_N = N_2\), \(((BD))_N = N_1\) and \(((AD))_N = ((BC))_N = 0\). We must find the coefficient \(A\), \(B\), \(C\), and \(D\) in (1) so that all values of \(n\) and \(k\) between 0 and \(N-1\) are unique and such that the twiddle factors disappear [12], [13].

\[
W^{(An_1 + Bn_2)}(Ck_1 + Dk_2) = W^{k_1n_2}_{N_1} \tag{1}
\]

### Table II

<table>
<thead>
<tr>
<th>INDEX AND RANGE FOR PRIME FACTOR MAPPING</th>
</tr>
</thead>
<tbody>
<tr>
<td>INDEX (n)</td>
</tr>
<tr>
<td>((An_1 + Bn_2)) (N_1)</td>
</tr>
<tr>
<td>((Ck_1 + Dk_2)) (N_2)</td>
</tr>
</tbody>
</table>

A. Uniqueness Condition

To find the uniqueness condition, the Chinese Remainder Theorem (CRT) is used. One set of coefficients that satisfies the uniqueness condition and eliminates the twiddle factor can be described as below.

\[
A = N_1, \quad B = N_1 \\
C = N_1((N_1^{-1}))N_1, \quad D = N_1((N_1^{-1}))N_1 \tag{2}
\]

The DFT is defined by

\[
X[k] = \sum_{n=0}^{N-1} x[n] \cdot W^{kn}_{N_1}, \quad k = 0, 1, \ldots, N-1 \tag{3}
\]

Using these index mappings, we can express the DFT as a function of the two indices \(k_1\) and \(k_2\). If we substitute (2) into (3), the DFT equation can be expressed as shown below.

\[
X[((N_2((N_2^{-1})k_1 + N_1((N_1^{-1}))k_1))k_2)] = \sum_{n_1=0}^{N_1-1} \sum_{n_2=0}^{N_2-1} x[n_1n_2] W^{n_1k_1}_{N_1} W^{n_2k_2}_{N_2} \tag{4}
\]
B. Middle Expression

The two dimensional array representation of the input is shown in Table III. Modulo N reduction is necessary for these index maps so that the effective values of n and k remain between 0 and N-1. The N-point transforms of the rows lead to the representation shown below.

\[
M[n_i, k_j] = \sum_{n_i=0}^{N_i-1} x((N_i n_i+N_j n_j)) \cdot W^{n_i k_j} \quad (5)
\]

<table>
<thead>
<tr>
<th>TABLE III</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Index 2D Expression</td>
</tr>
<tr>
<td>n_i</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>N_i-1</td>
</tr>
</tbody>
</table>

Since no twiddle factors are needed, the column transforms are given by

\[
X[((N_i (N_i^{-1}) n_i + N_j (N_j^{-1}) n_j)) x] = \sum_{n_i=0}^{N_i-1} M[n_i, k_j] \cdot W^{k_j n_i} \quad (6)
\]

Using (6) and considering DRM system needs 288, 256, 176, and 112 FFT sizes, the complexity of mixed prime factor FFT can be dramatically reduced by 32, 16, 11, 9, and 7 factors with sine and cosine coefficients; the maximum number of coefficients is 22.

III. PROPOSED PIPELINED MIXED PFA FFT

The proposed pipelined architecture of a mixed prime factor algorithm (PFA) for DRM mainly comprises a radix-2^n FFT module, one modified 11-point DFT module, and three shuffling modules, as shown in Fig. 4. The input shuffling module arranges the outputs of the input register block to provide proper CRT mapping for the radix-2^n FFT module and is comprised of multiplexers for proper routing of the outputs. A middle shuffling module is used to support the 4 different modes of the DRM system. It arranges the outputs of the radix-2^n FFT module to provide the proper inputs for the modified 11-point DFTs module using CRT mapping.

The 11-point DFT module is a combinational circuit, and the DFT is computed using a Winograd Fourier Transform Algorithm (WFTA) [8]. The implementation of the 11-point DFT is divided into 4 steps that correspond to the flow in the algorithm, as shown in Fig. 5. In the first step, stored values of middle register perform the switching for the second summation block. Several summations are calculated for the DFT in the second step. In the third step, the results of the second step are multiplied with 5 complex multipliers. In the last step, the final summations for DFT are calculated, and the results are stored in the D11 output register block in which output data is ordered by the shuffling module.

A. Expressions of PFA FFT for DRM

Using the extended pipeline architecture of the CRT mapping, the input, middle, and output data sequences can be directly loaded into 4 kinds of FFT points. More importantly, the CRT mapping can also be used to represent the output data, and the computed results should be stored in 3 kinds of shuffling registers. From (6), the proposed PFA FFT expressions with CRT mapping can be described as below.

\[
288 \text{ point : } X[((225k_i + 64k_j))_{288}] = \sum_{n_i=0}^{32} \left[ \sum_{n_j=0}^{32} x((9n_i + 32n_j))_{288} \right] W_{288}^{n_i k_i} \quad (7)
\]

\[
176 \text{ point : } X[((33k_i + 144k_j))_{176}] = \sum_{n_i=0}^{16} \left[ \sum_{n_j=0}^{16} x((11n_i + 16n_j))_{176} \right] W_{176}^{n_i k_i} \quad (8)
\]

\[
112 \text{ point : } X[((49k_i + 64k_j))_{112}] = \sum_{n_i=0}^{8} \left[ \sum_{n_j=0}^{8} x((7n_i + 16n_j))_{112} \right] W_{112}^{n_i k_i} \quad (9)
\]

Mixed PFA FFT calculates 32 points and 16 points using the radix-2 method. A pipeline radix-2^n structure is devised, and a multiplexer is used to distinguish 288, 256 points or 176, 112.
points. Because of the multiplying twiddle factor in 256 point, a complex multiplier is used between the radix-2<sup>n</sup> FFT module and the middle register. A multiplied twiddle factor results in a factor value for arithmetic and is stored in read-only memory (ROM).

### B. 11-point DFT Block

The 11-point DFT block calculates 4 kinds of DFT and multiplexing operation to distinguish the 7, 8, 9, 11 points. By using a multiplexer, 4 kinds of DFT points can be calculated without changing hardware. If the control signal indicates the use of the 11 point mode, values from a0 to a10 are received and multiplied by the twiddle factor. The 11-point DFT has a maximum twiddle factor parameter of 5. Because the input and output sequences are not in normal order, the elimination of the twiddle factor multiplications by the PFA is at the expense of complex indexing within the algorithm. In contrast to radix-2<sup>n</sup> algorithms, which use a single butterfly computation and a highly nested program structure, a PFA requires a different butterfly for each factor and is most easily programmed by taking one factor at a time. The radix-2<sup>3</sup> algorithm has the same computational complexity as the split-radix algorithm [17].

As shown in Fig. 6, the multiplicative operations are in such an arrangement that for every 3 columns, one has nontrivial full complex multiplication operation.

### C. Performance Analysis

For performance evaluation, the conventional structure and the proposed mixed PFA FFT structure are compared by the number of arithmetic operator units needed, such as multipliers and adders. The proposed mixed PFA FFT structure uses a multiplexer-based architecture to calculate radix-2<sup>n</sup> points. Such architecture decreases the total number of multipliers and adders. As shown in Tables IV and V, the total number of multipliers and adders are reduced by approximately 34.1% and 28.9%, respectively. From the comparison, we can conclude that proposed PFA FFT structure decreases the number of operator units and is excellent for area and power consumption.

### IV. CONCLUSION

In this paper, we proposed a mixed prime factor algorithm and an efficient architecture for DRM systems. For non-power-of-two FFTs, neither the input nor the output sequences are in normal order, and the mixed PFA FFT is chosen as the most attractive approach. From experimental results, it was shown that the proposed mixed PFA FFT can dramatically reduce the total number of multipliers and adders needed. The mixed PFA FFT requires less data storage memory, and the number of multiplications by different constants is much smaller than that in the other algorithm. As a result, the proposed architecture reduces the processing time and energy consumption of portable DRM receivers.

#### TABLE IV

<table>
<thead>
<tr>
<th>Point</th>
<th>PFA FFT</th>
<th>R2SDF</th>
<th>R4SDC</th>
<th>R2’SDF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mul</td>
<td>Add</td>
<td>Mul</td>
<td>Add</td>
<td>Mul</td>
</tr>
<tr>
<td>288</td>
<td>1000</td>
<td>5928</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>512</td>
<td>-</td>
<td>-</td>
<td>4096</td>
<td>9216</td>
</tr>
<tr>
<td>176</td>
<td>860</td>
<td>2688</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>256</td>
<td>-</td>
<td>-</td>
<td>1792</td>
<td>4096</td>
</tr>
<tr>
<td>112</td>
<td>396</td>
<td>2188</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>128</td>
<td>-</td>
<td>-</td>
<td>768</td>
<td>1792</td>
</tr>
</tbody>
</table>

#### TABLE V

<table>
<thead>
<tr>
<th>Point</th>
<th>PFA FFT</th>
<th>Real Multiplier</th>
<th>Adder</th>
</tr>
</thead>
<tbody>
<tr>
<td>288</td>
<td>22</td>
<td>28</td>
<td></td>
</tr>
<tr>
<td>256</td>
<td>22</td>
<td>28</td>
<td></td>
</tr>
<tr>
<td>176</td>
<td>26</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>112</td>
<td>18</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td>88</td>
<td>104</td>
<td></td>
</tr>
<tr>
<td>Proposed PFA</td>
<td>30</td>
<td>30</td>
<td></td>
</tr>
</tbody>
</table>

### REFERENCES


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